Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

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1.-11. (Canceled)

12. (Previously Presented) An integrated circuit, comprising:

an indium-fluorine retrograde well inside a substrate, the indium-fluorine retrograde well including an indium concentration greater than about 3E18/cm3.

13. (Previously Presented) The integrated circuit of claim 12, wherein the indium-fluorine retrograde well includes an indium concentration three times, or more, greater than 3E18/cm3.

14. (Previously Presented) The integrated circuit of claim 12, wherein the indium-fluorine retrograde well includes a fluorine concentration between about 5E18/cm3 to about 3E20/cm3.

15. (Previously Presented) The integrated circuit of claim 12, wherein the indium-fluorine retrograde well includes an indium concentration peak at about 200Å, or deeper, below the substrate surface.

16. (Original) An integrated circuit, comprising:

a substrate;

a gate structure formed on the substrate; and

an indium-fluorine retrograde well formed to a shallow depth below a surface of the substrate and beneath the gate structure.

17. (Original) The integrated circuit of claim 16, comprising an indium concentration above about 3E18.

18. (Previously Presented) The integrated circuit of claim 16, wherein the indium-fluorine retrograde well includes an indium concentration three times, or more, greater than 3E18/cm3.

19. (Previously Presented) The integrated circuit of claim 16, wherein the indium-fluorine retrograde well includes a fluorine concentration between about 5E18/cm3 to about 3E20/cm3.

20. (Original) The integrated circuit of claim 16, wherein the indium has a concentration peak at about 200Å, or deeper, below the substrate surface.

21. (Previously Presented) An integrated circuit, comprising:

a gate structure overlying a silicon substrate;

source/drain regions inside the silicon substrate, the source/drain regions adjacent to opposing sides of the gate structure and extending slightly underneath the gate structure; and

a fluorine-indium retrograde well directly beneath the gate structure and between the source/drain regions, the fluorine-indium retrograde well including an indium concentration greater than 3E18/cm3.

22. (Previously Presented) The integrated circuit of claim 21, wherein the fluorine-indium retrograde well is to provide a threshold voltage greater than about 360mV.

23. (Previously Presented) The integrated circuit of claim 21, wherein the fluorine-indium retrograde well includes an indium concentration peak at about 200Å, or deeper, below the substrate surface.

24. (Previously Presented) The integrated circuit of claim 21, wherein the gate structure has a gate length of about 60nm or less.

25. (Previously Presented) The integrated circuit of claim 21, wherein the fluorine-indium retrograde well includes an indium concentration three times, or more, greater than 3E18/cm3.